IN THE CLAIMS

Please cancel claims 20-42 without prejudice.

Please amend the following claims.

1. (Currently amended) A semiconductor device comprising:

a semiconductor body on a bulk semiconductor substrate, said semiconductor body having a top surface and laterally opposite sidewalls;

a semiconductor capping layer formed on the top surface and on the sidewalls of said semiconductor body;

a gate dielectric layer formed on said semiconductor capping layer on said top surface and on said sidewalls of said semiconductor body;

a gate electrode having a pair of laterally opposite sidewalls formed on and around said gate dielectric layer; and

a pair of source/drain regions formed in said semiconductor body on opposite sides of said gate electrode.

2. (Original) The semiconductor device of claim 1 wherein said semiconductor capping layer have a tensile stress.

3. (Currently amended) The semiconductor device of claim 2 wherein said semiconductor capping layer has greater tensile stress on the sidewalls of said semiconductor body ~~and then~~ than on the top surface of said semiconductor body.

4. (Original) The semiconductor device of claim 2 wherein said source/drain regions are n type conductivity.

5. (Currently Amended) The semiconductor device of claim 1 wherein said bulk semiconductor substrate is a silicon substrate, wherein said semiconductor body is a silicon germanium alloy and wherein said semiconductor capping layer is a silicon film.

6. (Original) The semiconductor device of claim 1 wherein said semiconductor capping layer has a compressive stress.

7. (Original) The semiconductor device of claim 6 wherein said semiconductor capping layer has a greater compressive stress on the sidewalls than on the top surface of said semiconductor body.

8. (Currently amended) The semiconductor device of claim 6 wherein said bulk semiconductor substrate is a monocrystalline silicon substrate, wherein said semiconductor body comprises a silicon-carbon alloy and wherein said semiconductor capping is a silicon film.

9. (Currently amended) The semiconductor device of claim 1 wherein said bulk semiconductor substrate is a silicon substrate, wherein said semiconductor body is a silicon-carbon alloy ~~body~~, and wherein said semiconductor capping layer is a silicon capping layer.

10. (Currently amended) A semiconductor device comprising:

a silicon germanium body formed on a bulk silicon monocrystalline substrate, said silicon germanium body having a top surface and a pair of laterally opposite sidewalls;

a silicon film formed on said top surface and on said sidewalls of said silicon germanium body;

a gate dielectric layer formed on said silicon film on said top surface of said ~~semiconductor~~ silicon germanium body and on said silicon film on said sidewalls of said ~~semiconductor~~ silicon germanium body;

a gate electrode having a pair of laterally opposite sidewalls formed on and around said gate dielectric layer; and

a pair of source/drain regions formed in said ~~semiconductor~~ silicon germanium body on opposite sides of said gate electrode.

11. (Currently amended) The semiconductor device of claim 10 wherein said silicon film is formed thicker on the top surface of said ~~semiconductor~~ silicon germanium body than on the sidewalls of said semiconductor body.

12. (Original) The semiconductor device of claim 10 wherein said silicon film has a thickness between 50-300Å.

13. (Original) The semiconductor device of claim 10 wherein said silicon germanium alloy comprises between 5-40% germanium.

14. (Original) The semiconductor device of claim 13 wherein said silicon germanium alloy comprises approximately 15-25% germanium.

15. (Original) The semiconductor device of claim 10 wherein said source/drain regions are n type conductivity.

16. (Currently amended) A semiconductor device comprising:

a silicon-carbon alloy body formed on a silicon monocrystalline substrate, said silicon carbon alloy body having a top surface and a pair of laterally opposite sidewalls;

a silicon film formed on said top surface and on said sidewalls of said silicon carbon alloy body;

a gate dielectric layer formed on said silicon film on said top surface of said silicon-carbon body and on said silicon film on said sidewalls of said silicon-carbon alloy body;

a gate electrode having a pair of laterally opposite sidewalls formed on and around said gate dielectric layer; and

a pair of source/drain regions formed in said ~~semiconductor~~ silicon carbon-alloy body on opposite sides of said gate electrode.

17. (Original) The semiconductor device of claim 16 wherein said silicon film is formed to a thickness between 50-300Å.

18. (Original) The semiconductor device of claim 17 wherein said silicon film has a thickness between 50-300Å.

19. (Original) The semiconductor device of claim 16 wherein said source/drain regions are p type conductivity.

20.- 42.(Canceled)

43. (New) A semiconductor device comprising:

a silicon germanium body formed on a silicon monocrystalline substrate, said silicon germanium body having a top surface and a pair of laterally opposite sidewalls;

a silicon film formed on said top surface and on said sidewalls of said silicon germanium body, wherein said silicon film is formed thicker on the top surface of said silicon germanium body than on the sidewalls of said semiconductor body;

a gate dielectric layer formed on said silicon film on said top surface of said silicon germanium body and on said silicon film on said sidewalls of said silicon germanium body;

a gate electrode having a pair of laterally opposite sidewalls formed on and around said gate dielectric layer; and

a pair of source/drain regions formed in said silicon germanium body on opposite sides of said gate electrode.

44. (New) A semiconductor device comprising:

a semiconductor body on a bulk semiconductor substrate, said semiconductor body having a top surface and laterally opposite sidewalls, wherein said semiconductor body is comprised of a material which has a different lattice constant than said bulk semiconductor substrate;

a semiconductor capping layer formed on the top surface and on the sidewalls of said semiconductor body, wherein said semiconductor capping layer comprises a material which has a different lattice constant than said semiconductor body;

a gate dielectric layer formed on said semiconductor capping layer on said top surface and on said sidewalls of said semiconductor body;

a gate electrode having a pair of laterally opposite sidewalls formed on and around said gate dielectric layer; and

a pair of source/drain regions formed in said semiconductor body on opposite sides of said gate electrode.

45. (New) The semiconductor device of claim 44, wherein said semiconductor body comprises a material having a lattice constant that is larger than the lattice constant of said bulk semiconductor substrate.

46. (New) The semiconductor device of claim 44, wherein said semiconductor body comprises a material having a lattice constant that is smaller than the lattice constant of said bulk semiconductor substrate.

47. (New) The semiconductor device of claim 44, wherein said semiconductor capping layer comprises a material having a lattice constant that is larger than the lattice constant of said semiconductor body.

48. (New) The semiconductor device of claim 44, wherein said semiconductor capping layer comprises a material having a lattice constant that is smaller than the lattice constant of said semiconductor body.

49. (New) The semiconductor device of claim 44, wherein said bulk semiconductor substrate is a silicon substrate, wherein said strained semiconductor body is a silicon germanium alloy and wherein said semiconductor capping layer is a silicon film.

50. (New) The semiconductor device of claim 44, wherein said bulk semiconductor substrate is a silicon substrate, wherein said strained semiconductor body is a silicon-carbon alloy body, and wherein said semiconductor capping layer is a silicon capping layer.

51. (New) A semiconductor device comprising:

a strained semiconductor body on a bulk semiconductor substrate, said strained semiconductor body having a top surface and laterally opposite sidewalls;

a semiconductor capping layer formed on the top surface and on the sidewalls of said strained semiconductor body;

a gate dielectric layer formed on said semiconductor capping layer on said top surface and on said sidewalls of said strained semiconductor body;

a gate electrode having a pair of laterally opposite sidewalls formed on and around said gate dielectric layer; and

a pair of source/drain regions formed in said strained semiconductor body on opposite sides of said gate electrode.